Development of Cryogenic Load-Pull Analysis: Power Amplifier Technology Performance Trends

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ABSTRACT

On-wafer load-pull measurements at cryogenic temperatures are made for the first time on FET power amplifier structures to demonstrate the improved performance when operated at reduced temperatures. Measurements from 300K to 17K demonstrate improvements in both efficiency (40-80 %) and output power (1.0-2.7 dB). These results demonstrate that advanced device technologies that are optimized for cooled operation may provide significantly enhanced system performance and reliability with a minimal increase in prime power.

INTRODUCTION

High-radiated power solid state phased array radar systems are in demand for their improved sensitivity. High power amplifiers (HPAs) are the most important components in the T/R modules[1]. Current state of the art P-HEMT GaAs power devices are capable of 0.5-0.7 W/mm of gate width at 300K at a cost of about $10-$15/mm. Alternative methods for increasing radiated power are desirable and one method is by decreasing the physical temperature of existing HPAs.

The performance of solid state phased array radar may be significantly improved by operating at reduced lattice temperatures. Even, moderate cooling has the potential to provide significant performance enhancements to several key hardware elements including: T/R modules, power supplies, and higher level assemblies.

At the device level, reduced temperature operation holds the promise of higher power and efficiency. For the module level, reduced temperature operation has the potential for improved mean-time-to-failure (MTTF).

In this paper we:

- Demonstrate the feasibility of cryogenic on-wafer load-pull analysis
- Demonstrate the first on-wafer cryogenic load-pull characterization of microwave transistors
- Provide formulations for comprehensive device level studies of important technologies for power amplifier applications

EXPERIMENT

We have adapted the on-wafer cryogenic measurement technique[2] to an ATN load-pull system. This new system allows temperature (300-20 K) and bias dependent power measurements for complete load-pull analysis. The measurement reference planes are established directly at the device under test

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(DUT). This condition is achieved through a set of user calibrations: Short-Open-Load (SOL), Power Transfer, 2 port S-parameter and Thru delay. The calibration was validated by measuring a 50-ohm Thru. Additionally, for measurement accuracy, the calibrations are performed at each temperature of interest: 300K, 200K and 20K[3]. This measurement approach provides the foundation for developing microwave large signal models over a wide temperature range and represents a significant contribution to recently reported approaches for temperature dependent large signal models [4].

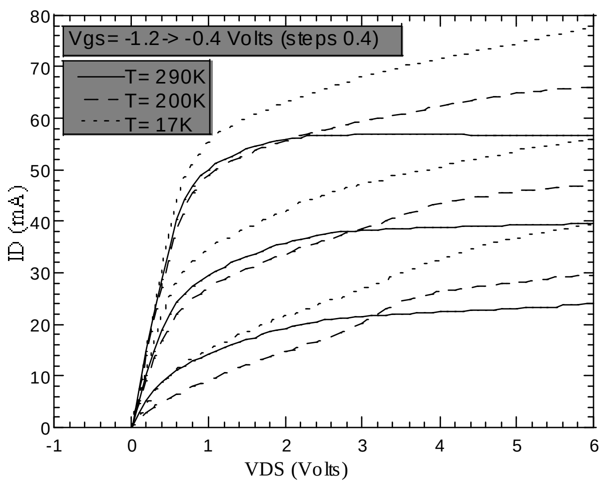

Figure 1: GaAs MESFET (Lg=0.6 µm, W=300 µm) Drain Current curves at 290K, 200K and 17K

RESULTS

Four different devices, two GaAs MESFET with Lg=0.6µm but different Width 200, 300 µm, an $In_{65}Ga_{35}As/InP$ HEMT with Lg=0.1µm, and a GaAs-based P-HEMT with Lg=0.25µm have been characterized.

In Figure 1, we show the influence of temperature on the drain current and drain voltage characteristics of the GaAs MESFET with W=300µm. The decrease in the physical temperature of the device results in an increase in both the MESFET electron mobility and carrier channel velocity which results in an increase in the device transconductance[5].

In figure 2 and 3, we show the effect of temperature (290-17 K) on Contour Circles of Constant Efficiency and Output Power for the GaAs MESFET (W=300µm) sample. The input impedance was set for maximum small signal gain and the input power was set at the 1dB compression point. The decrease in temperature results in larger contour circles for that same condition of constant Efficiency and Output Power at room temperature. An improvement in the Efficiency and the Output Power with the physical decrease in the temperature of the device will result independently of the termination due to the fact that the same termination is now on a different contour circle with a higher Efficiency or Output Power. Figure 4 shows that result into 50-ohm termination for that same device.

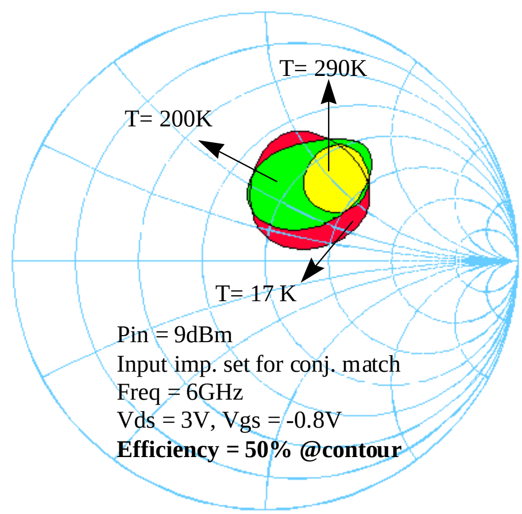

Figure 2: GaAs MESFET constant Efficiency Contour Circles for three different temperatures

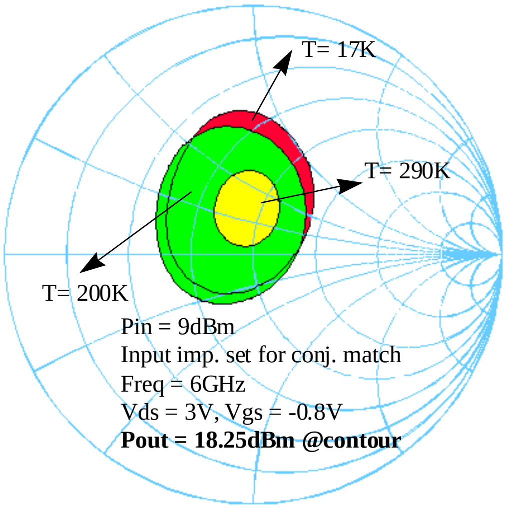

Figure 3: GaAs MESFET Constant Output Power Contour Circles for three different temperatures

In Figures 4-7, we show the effect of temperature (300-17 K) on power measurements into 50-ohm termination for the four discrete devices. In table 1, we summarize the increase in efficiency and the corresponding improvement in output power from 300K to 200K to 20K.

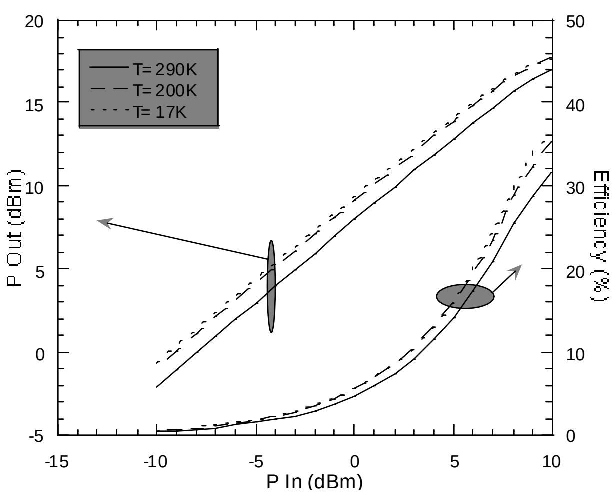

Figure 4: GaAs MESFET 6GHz (Lg=0.6µm, W=300µm) and Efficiency versus input power levels at 290K, 200K and 17K into 50 ohm termination. Vds=3V Vgs=-0.8V

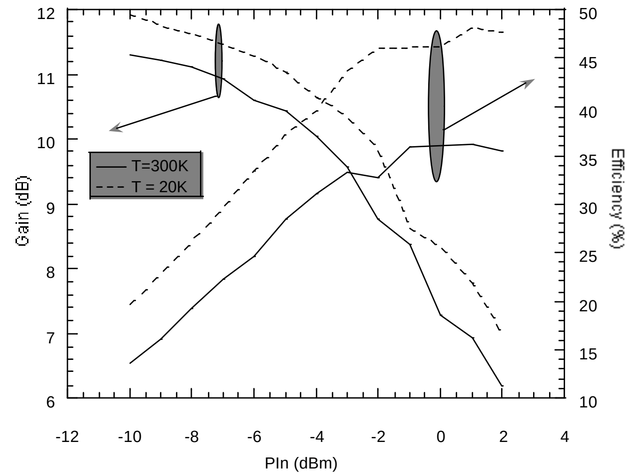

Figure 5: InP HEMT 10GHz Gain and Efficiency versus input power levels at 300K and 20K into 50-ohm termination. Vds=1V, Vgs=-0.1V

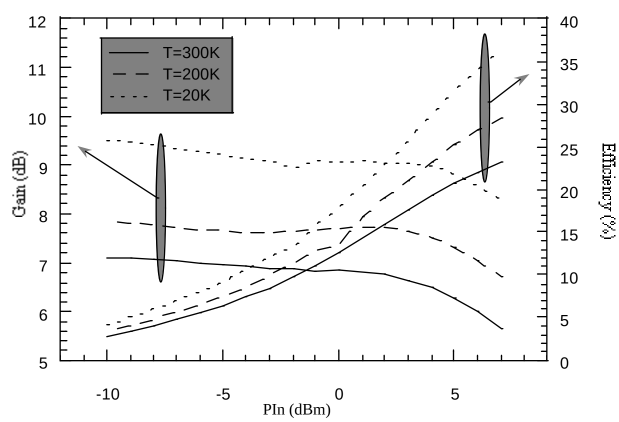

Figure 6: GaAs-based P-HEMT 8GHz Gain and Efficiency versus input power levels at 300K, 200K and 20K into 50 ohm termination at Vds=3V, Vgs=-0.8V

An initial large signal model for the GaAs MESFET (W=200µm) was implemented in MDS for both 300K and 20K operation. Figure 5 shows good agreement between measured and modeled data. Currently, we are developing detailed bias and temperature dependent models for MESFET, HEMT and PHEMT structures.

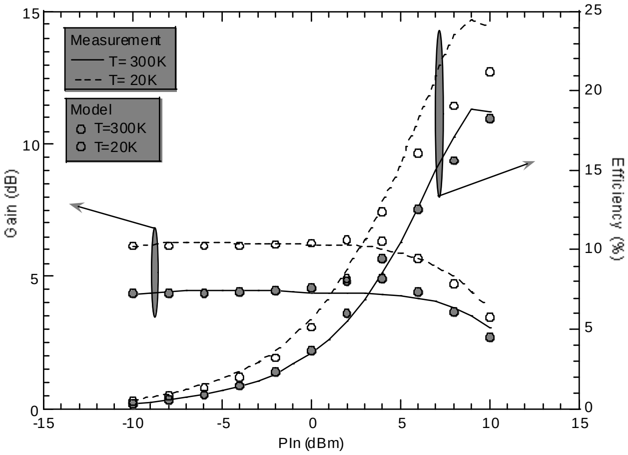

Figure 7: GaAs MESFET 10GHz measured, modeled Gain and Efficiency versus input power levels at 300K and 20K into 50 ohm termination at Vds=2V, Vgs=-0.8V

CONCLUSION

In summary, we have developed the first cryogenic on-wafer load-pull measurement system. This system has been employed to study the effect of temperature on several power amplifier device technologies: GaAs MESFET, GaAs PHEMT and InP HEMT. All device technologies exhibited significant increases in gain and efficiency as the physical temperature of the devices is lowered from 300K to 17K. An initial large signal model for the GaAs MESFET has been implemented and detailed models for MESFET, HEMT and PHEMT are under development.

ACKNOLEDGEMENTS

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Device	Freq.	Bias	variation in temp (K)	Pin (dBm)	% increase in Efficiency	corresponding improvement in Output Power (dB)
GaAs-based P-HEMT	8GHz	Vds=3 Vgs=-0.8	300-200	10	39.1	1.34
			300-20	10	78.2	2.73
InP HEMT	10GHz	Vds=1 Vgs=-0.1	300-20	0	43.0	1.07
GaAs MESFET (W=200μm)	10GHz	Vds=2 Vgs=-0.8	300-20	0	62.9	1.8

Table 1: Summary of the measured increases in efficiency and gain when reducing the operating temperature from 300K to 200K to 20K. These results are for 50-ohm termination conditions.